MENTOR GRAPHICS

IC DESIGN MANUAL

Schematic & Simulation

By

Gun Jun
K Praveen Jayakar Thomas
Zheng Huan Qun

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Signal Processing & VLSI Design Laboratory
Department of Electrical & Computer Engineering
National University of Singapore

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1. Invoking Design Architect – IC

After login, right click anywhere on the screen and select, ***Host*** > ***This Host*** to open a terminal window. Type the following to make a directory named "Lab_Training" and to change the working directory to it,

mkdir Lab_Training

cd Lab_Training

Invoke Design Architect-IC (DA-IC) by typing,

source /app11/mentor/cshrc.mentor

da_ic

click OK to the "What's New in Design Architect – IC" window.

2. Creating a Schematic

From the top left corner of the DA-IC window select ***MGC*** > ***Setup***. Click the ***Session*** tap and enable the following: ***Show Palette, Show Softkey Area, Show Symbol Window***. On pressing OK the DA-IC window will appear as in Fig 2.1.

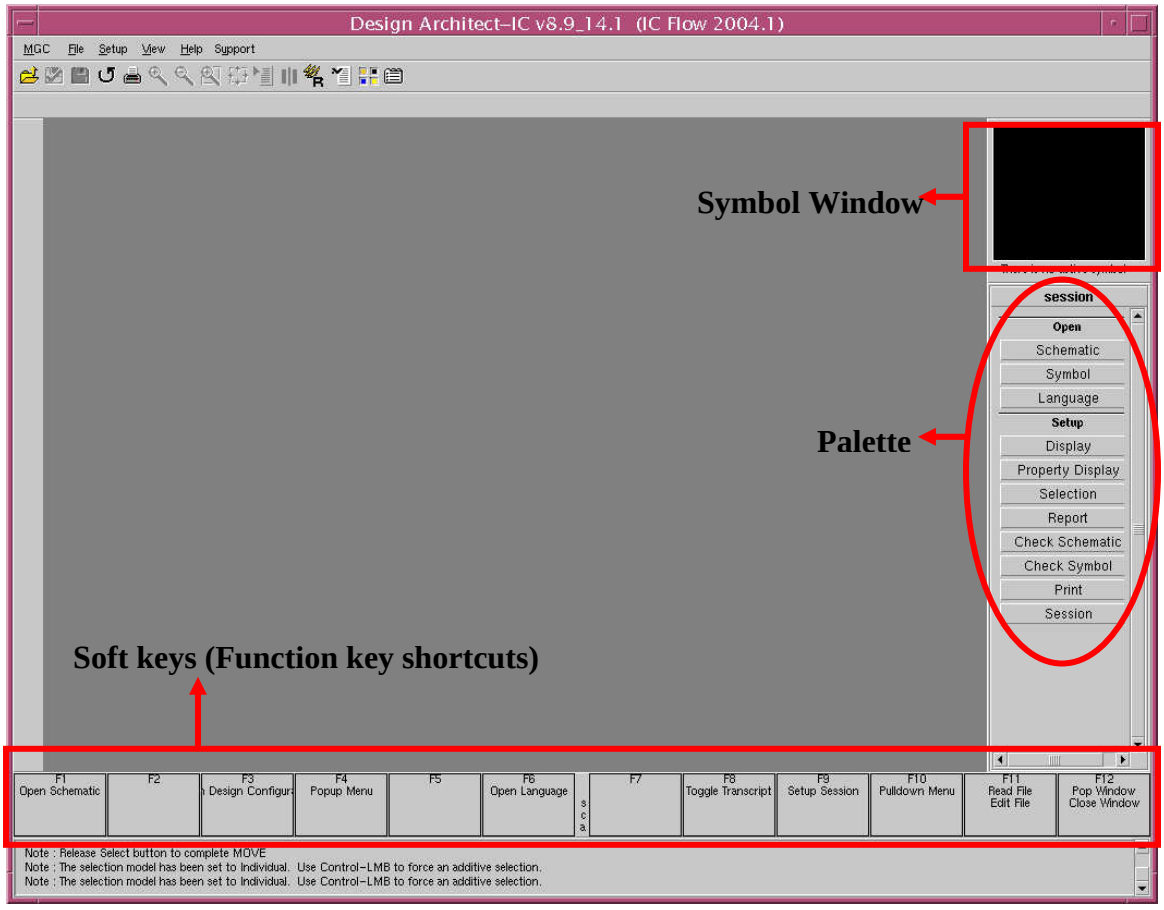


Figure 2.1 DA-IC window at start up.

Click ***Open*** - ***Schematic*** from the ***Session*** palette, which opens the Open Schematic dialog box. Fill in the component field as shown in Fig 2.2. Click ***Options***, in the form that follows check ***New Sheet*** and fill in the ***Sheet*** field has opamp_sch as shown in Fig.2.3.

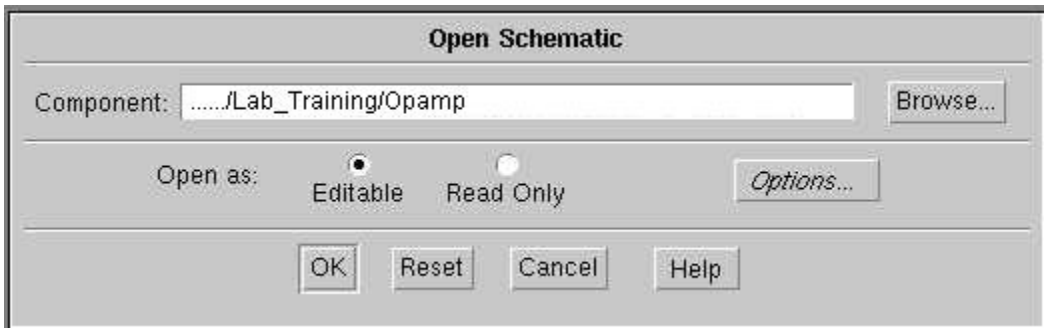


Figure 2.2 Opening a new schematic

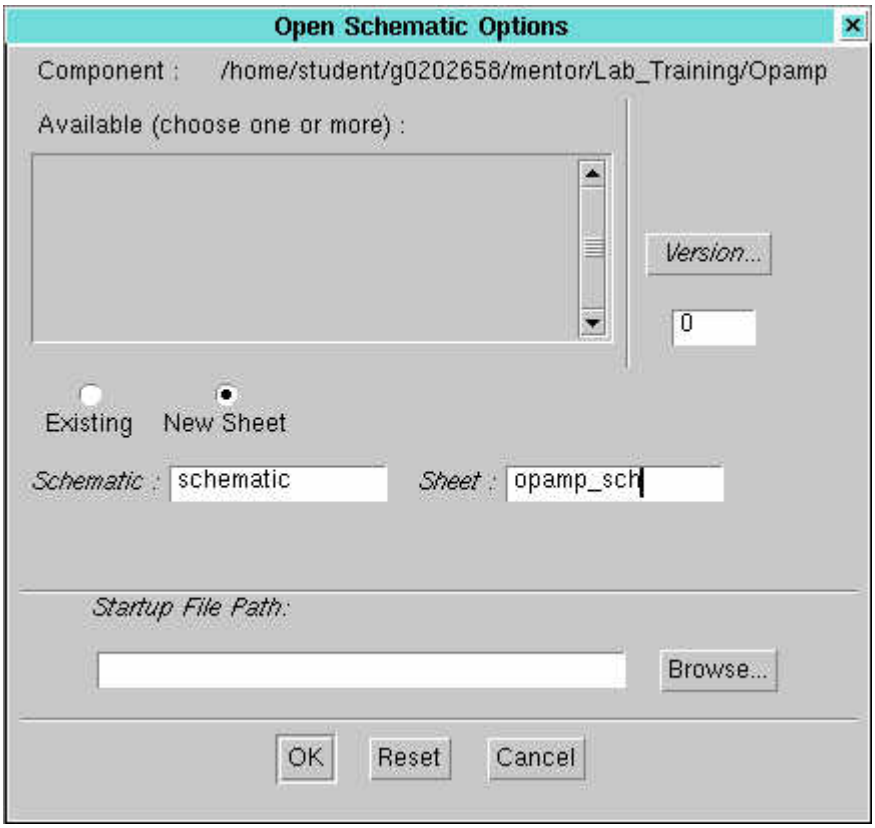


Figure 2.3 Opening a new schematic sheet

On pressing OK to the above two forms, DA-IC will create a Mentor Graphics Component object called “Opamp” and a new sheet file inside the component object called “opamp_shc” in the “Lab_Training” directory.

A new blank ***Schematic #1 Opamp opamp_sch*** workspace appears and the right hand side palette changes to a ***schematic edit*** palette. Follow the steps given below to create a schematic as shown in Fig. 2.4.

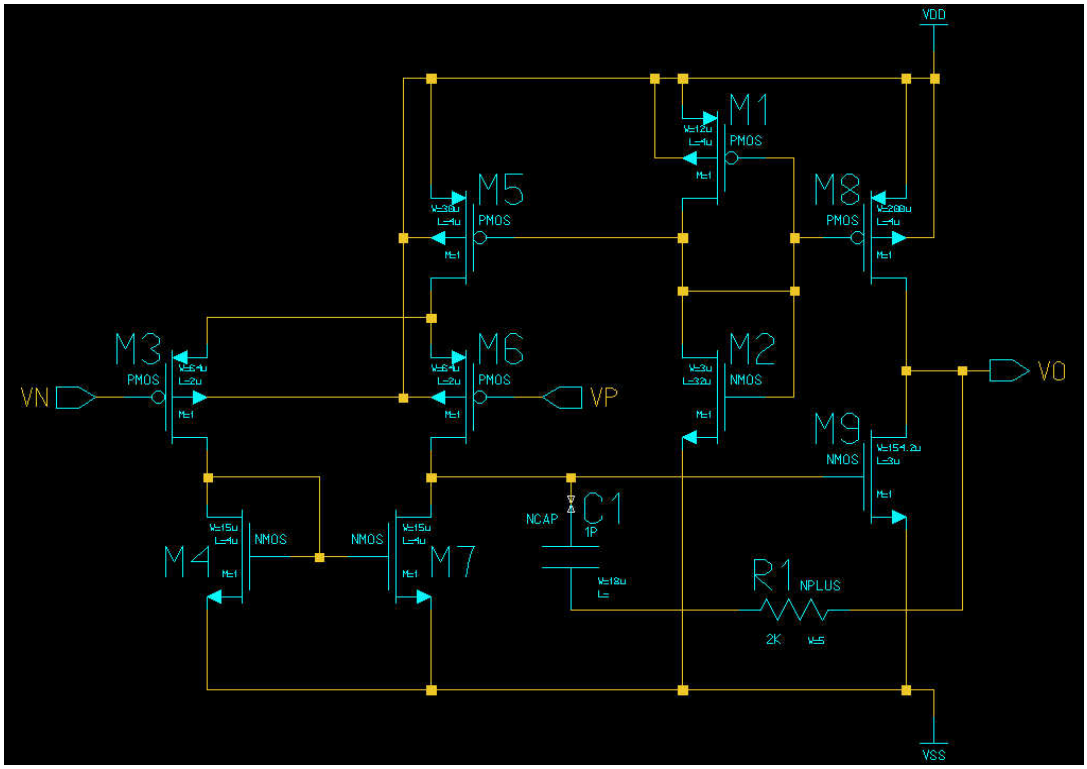
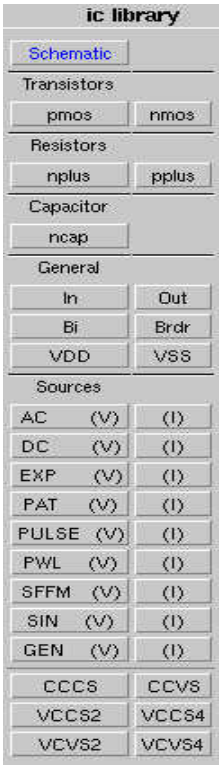


Figure 2.4 Schematic of the Opamp



Step 1 - Placing devices on the schematic

Click ***Library*** in the ***schematic_edit*** palette. This will open the ***ic library*** palette as shown beside, from which device selections are made. Place transistors on the schematic as in Fig. 2.4 by clicking ***Transistors pmos*** (or ***nmos***) with the left mouse button, then clicking anywhere in workspace. ***Resistors*** (***nplus*** and ***pplus***) and ***capacitors*** (***ncap***) are placed in the same manner. Note that as soon as you click a device in the ***ic library*** palette, its corresponding symbol appears in the symbol window (upper right side as explained in Fig 2.1). Click and place the input/output port from ***General In/Out*** and the supplies from ***General VDD/VSS***. To make space, use the ***View>Zoom In/ Zoom Out*** from the top menu bar or with the middle mouse button draw a upward/downward slant stroke (refer to the figures on right). Many short cuts are available with the middle mouse button stroke, to get help, draw a question mark with the middle mouse button anywhere on the workspace.

Step 2 – Selecting and editing the devices

After placing all the devices click ***schematic*** from the ***ic library*** palette to return to ***schematic edit*** palette. Any device can be selected with the left mouse button or by pressing F1 function key while the mouse pointer is over the device. After selecting the device use ***Edit*** section (shown beside) of the ***schematic edit*** palette to copy, delete, flip etc. the devices (editing can also be done with middle mouse button strokes). Click ***properties*** in the ***Edit*** section to change the W/L value of the transistors or the value of capacitors and resistors in accordance with the table given below.

Transistor	M1	M2	M3	M4	M5	M6	M7	M8	M9
W(u)/L(u)	12/4	3/32	64/2	15/4	30/4	64/2	15/4	200/4	154.2/3
Resistor	R1: ASIM_MODEL = NPLUS; R=2K; W=5								
Capacitor	C1: ASIM_MODEL = NCAP; c = 1P								

Step 3 – Routing the devices and naming the nets

Click ***Wire*** from the ***Add*** section of ***schematic edit*** palette to wire all the devices together as shown in Fig. 2.4. To start a wire, click once with the left mouse button and to end the wire double click the same button. After routing, click the wire that connects the transistor M6 and input port as shown in Fig. 2.4, then click ***Net*** from the ***Name*** section of ***schematic edit*** palette (if the ***Name*** section is not visible right click anywhere in the ***schematic edit*** palette and select ***Show Scroll Bars*** to get the scroll bars, using which the ***Name*** section can be located). In the form that pops up at the bottom of the window change the default name 'NET' in the New Value field by typing 'VP'. Name all the other ports in the same manner. Any net (wire) can also be named following the above procedure.

Save the above schematic by clicking ***Check & Save*** in the ***schematic edit*** palette.

3. Creating a Symbol

It is necessary to create a symbol for the above saved schematic sheet, so that it can be instantiated (placed) in other top level schematic sheets.

From the top menu bar pull down ***Miscellaneous*** > ***Generate Symbol***, click ***chooses shape*** from the dialog box that appears. Select ***Buffer*** and click OK to all the forms. A symbol with In/out port appears and the palette changes to ***symbol draw***. Click ***Text*** to change the palette to ***symbol text***. Place the mouse pointer over the text 'VN' and press F1 function key to select it. Click ***Text Attributes*** from ***Edit*** section of ***symbol text***

palette. Change the ***height*** to 0.4 in the Modify Property form. Click Ok and move the text 'VN' (by click and drag) to a position as shown in Fig. 3.1. Edit the symbol in the same manner to reflect Fig. 3.1. Save the symbol created by clicking ***Check & Save*** from the ***symbol text*** palette.

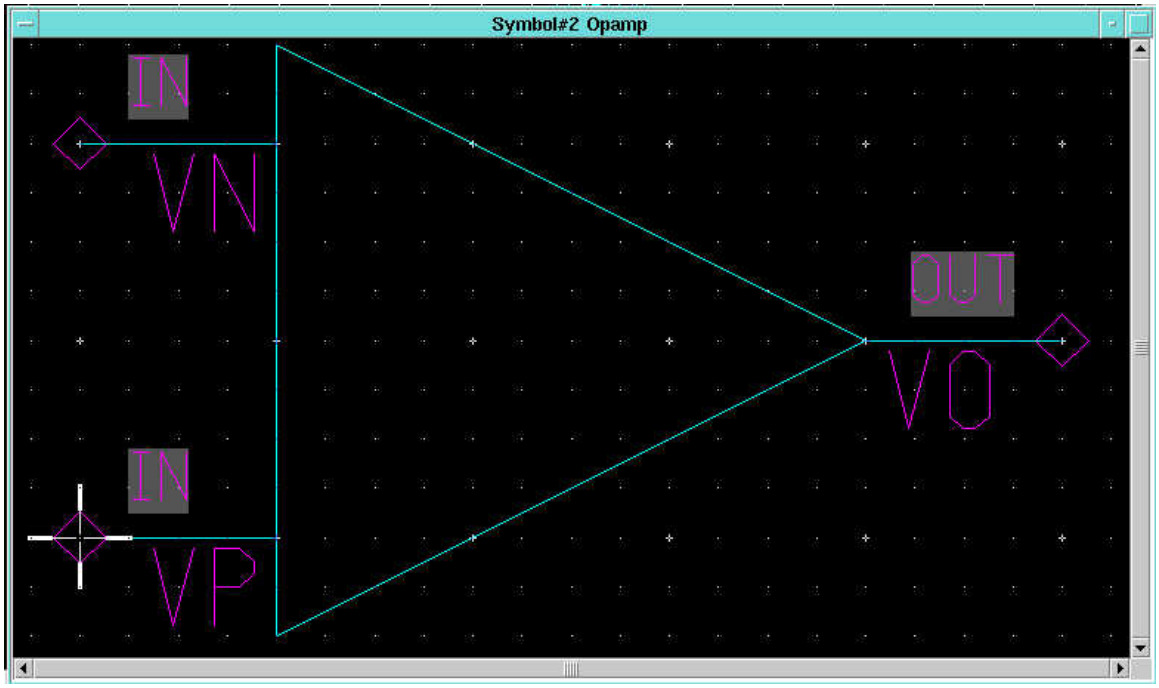


Figure 3.1 Creating a Symbol

4. Creating the Test bench

Step 1 Close all active schematic/symbol sheets. From the ***session*** palette click ***Schematic***. In the Open Schematic dialog box fill the component field as "…../Lab_Training/Opamp_Test" click ***Options***, select ***New Sheet*** and name the ***Sheet*** as "opamp_test_sch".

Step 2 Select ***Add - Instance*** in the ***schematic edit*** palette, browse to get the opamp symbol under '…../Lab_Training/Opamp', then click anywhere in the empty workspace to place the symbol.

Step 3 Open down into the opamp symbol and view the sub circuit by using the middle mouse button down stroke while the mouse pointer is over the instance. Verify that the schematic contains a transistor level description of the functionality. Use the open up feature to return to the main schematic with the up-then-to-the-right stroke (refer to the figure on right).

Step 4 Select ***Library*** to change the palette to ***ic library***. Place all the components needed to build a test bench as shown in Fig. 4.1. Click ***Schematic*** to return to ***schematic edit*** palette.

Step 5 Select the components one by one and ***Edit - Properties*** to match the values given in the table below.

V1 : DC = 1.5V	Resistor : R = 100K ASIM_MODEL = NPLUS W = 3
V2 : DC = 1.5V mag = 1V phase = 0	
V3 : DC = 3.3V	

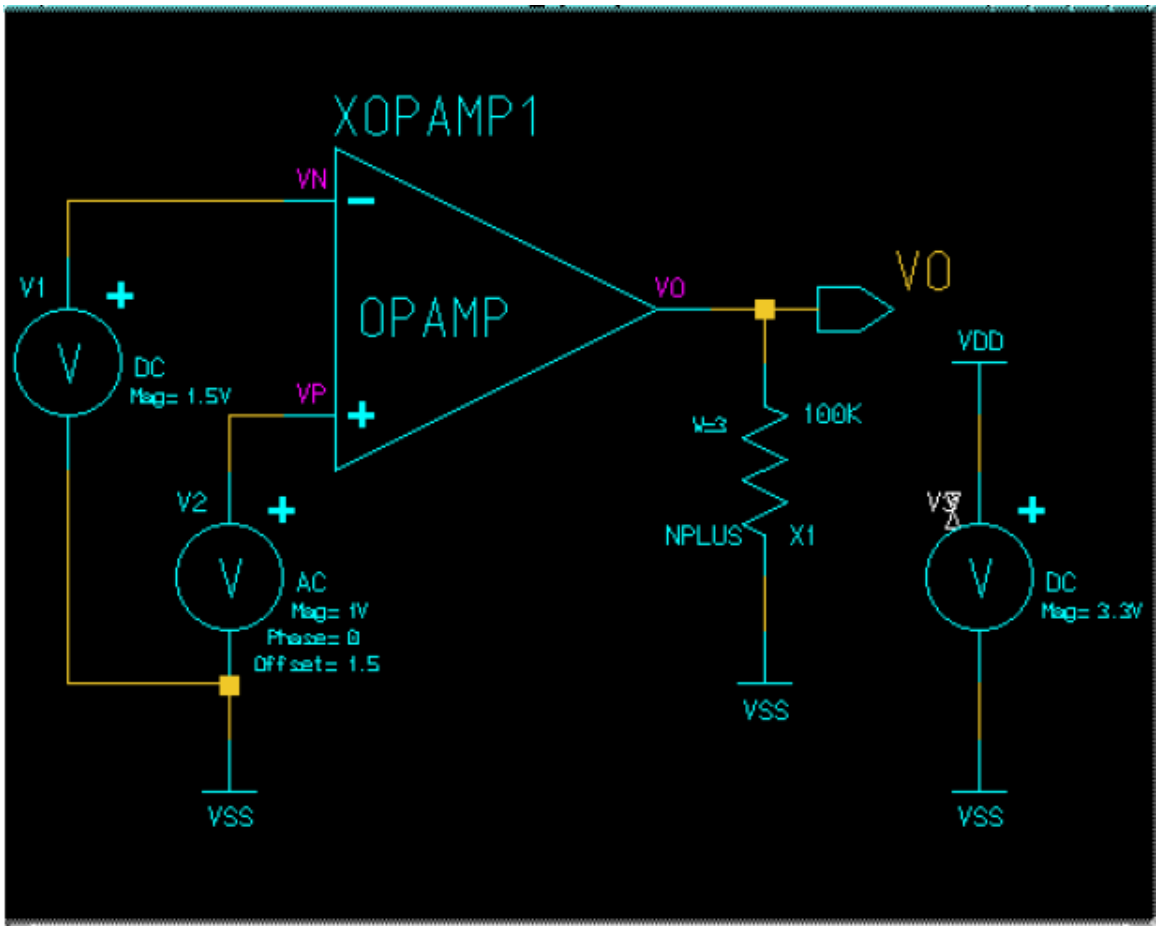


Figure 4.1 Creating a Test bench

Step 6 Add an output port and name it 'VO', route the schematic as shown in Fig. 4.1. ***Check & Save*** the test bench.

5. Running an Analog Simulation

In previous sections, we created a schematic of a differential opamp and used that schematic to create a higher level symbol of the opamp circuit. Then we set up a testbench to test our opamp design. Now we're ready to run an analog simulation of that design using Eldo.

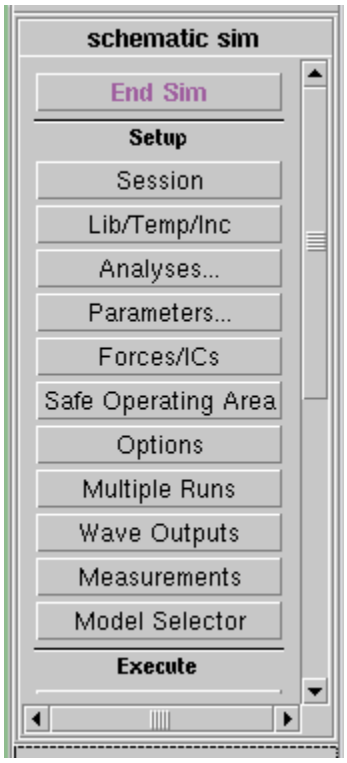
5.1 Enter Simulation Mode

Click ***Simulation*** in the **schematic_edit** palette and click OK in the "Entering Simulation mode" dialog box. Now the circuit is under simulation mode. The program will save all schematics that are open, then creating a design viewpoint called **eldonet** that is automatically created for the EldoNet application.

When editing in this mode, only a subset of the normal Design Architect-IC editing functions are available because certain Design Architect-IC editing methodologies, such as editing symbols in place and updating those symbols on the schematic, adversely affect the design as it is stored in memory.

5.2 Setup the Simulation

We'll use the Setup options on the **schematic_sim** palette to setup the simulation commands.



Step 1 Select ***Setup*** > ***Session*** > ***Netlister*** and set Node 0 = VSS.

By setting "Node 0", we are telling the Eldo simulator which net names are to be considered as ground.

Click OK to accept any changes.

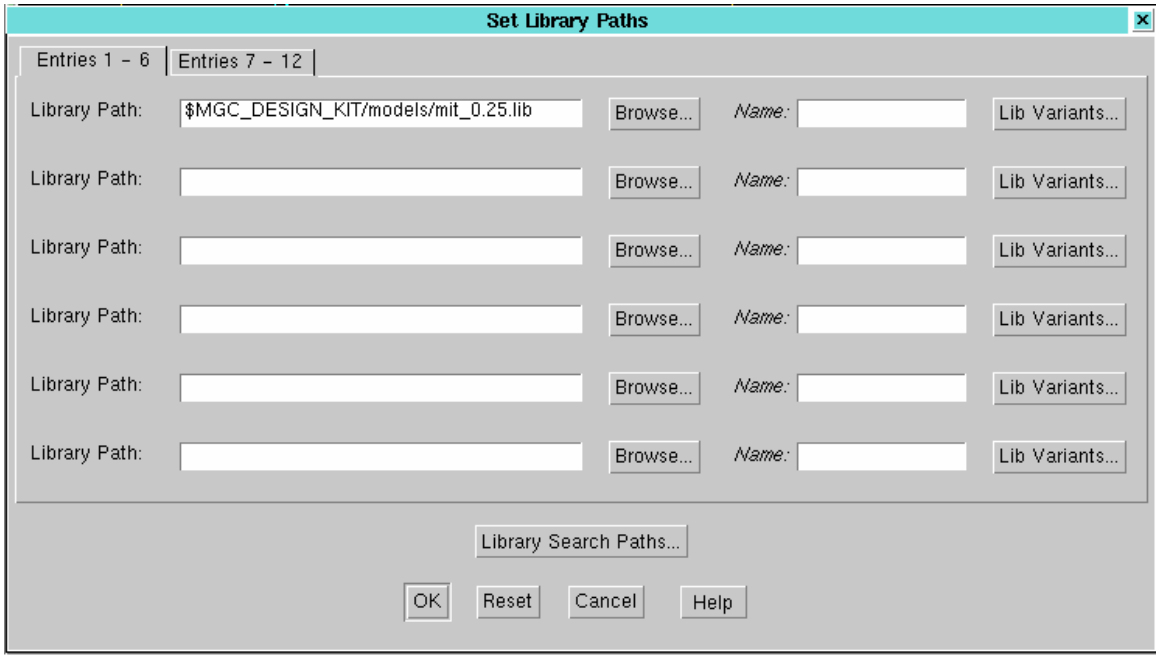
Step 2 Click ***Setup*** > ***Session*** > ***Simulator/Viewer***.

Choose simulator to be **Eldo** and viewer to be **Xelga**.

Click OK to accept any changes and close the dialog box.

Step 3 Click ***Setup*** > ***Lib/Temp/Inc*** > ***Libraries*** and use the browse button in the **Set Library Paths** dialog box to the following library path:

$MGC_DESIGN_KIT/models/mit_0.25.lib



In this command, we are specifying the pathnames to the ASCII SPICE model files used in the design. These contain foundry-specific models where the primitive components such as NMOS and PMOS transistors and diodes for a particular design process are formally defined using '.MODEL' statements.

Click OK to accept any changes and close the dialog box.

5.3 AC Analysis

Click ***Setup*** > ***Analyses*** and then click the Setup button for AC. In the "Setup AC Analysis" dialog box, set the following parameters:

Start Freq = 1MEG
Stop Freq = 1G
Points per Decade = 1000

Ok the dialog box.

Enable AC analysis by checking the box before AC in the "Setup Simulation Analysis" dialog box.

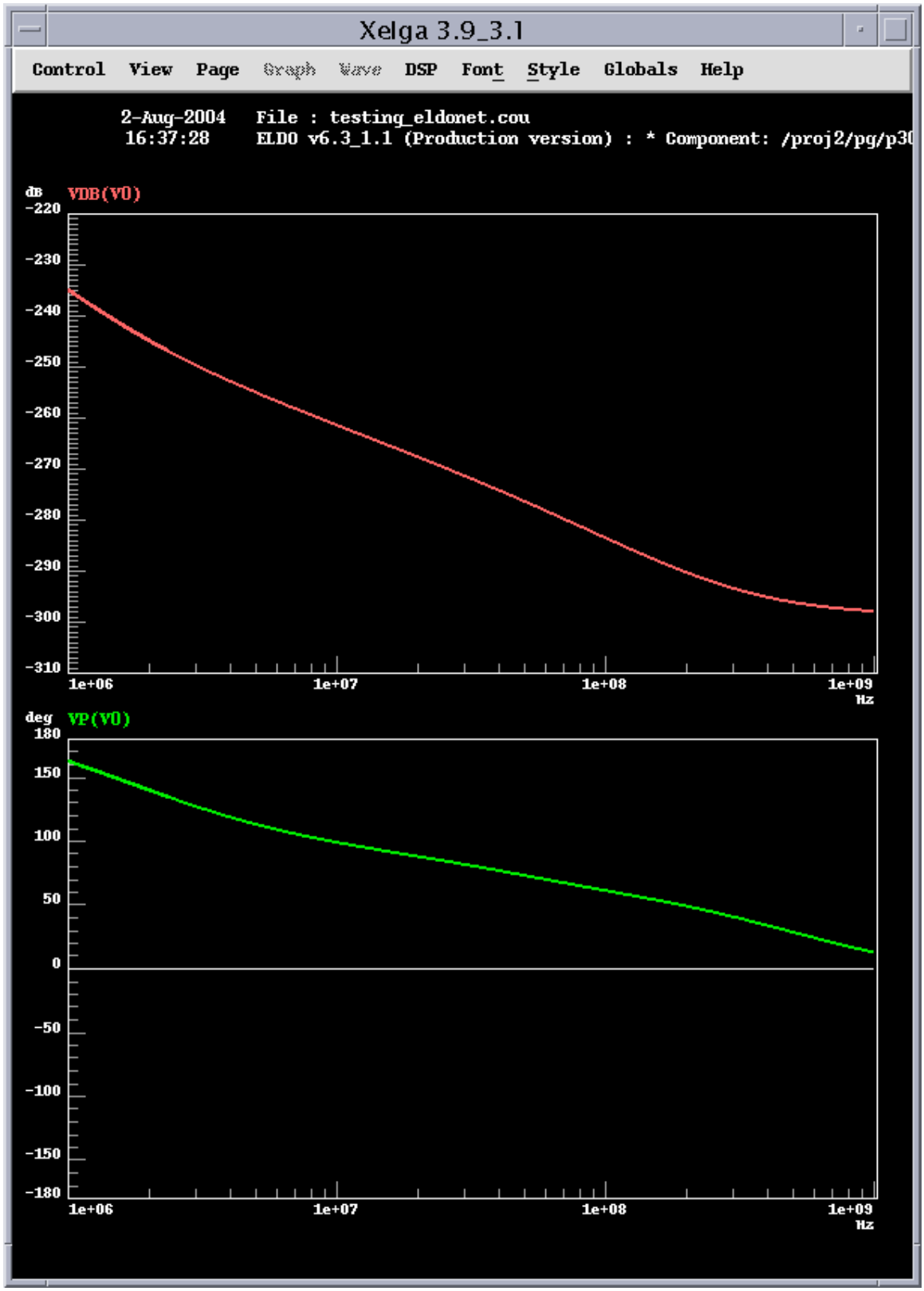
Click the V0 net and then right-click the wire, choose ***simulation*** **>** ***save & plot voltage*** **>** ***DB***. Right click again and choose ***PHASE***.

Click ***Setup*** **>** ***Session*** **>** ***Show Settings Block***, the information shown here indicates what analyses will be done.

Now click ***Execute*** **>** ***Run ELDO*** in the **schematic_sim** palette to run the simulation. By clicking that button, it generates the netlist first and then runs the simulation. Check any errors in the two popup windows.

You can now view the output waveforms by clicking ***Results*** **>** ***View Waves*** in the **schematic_sim** palette.

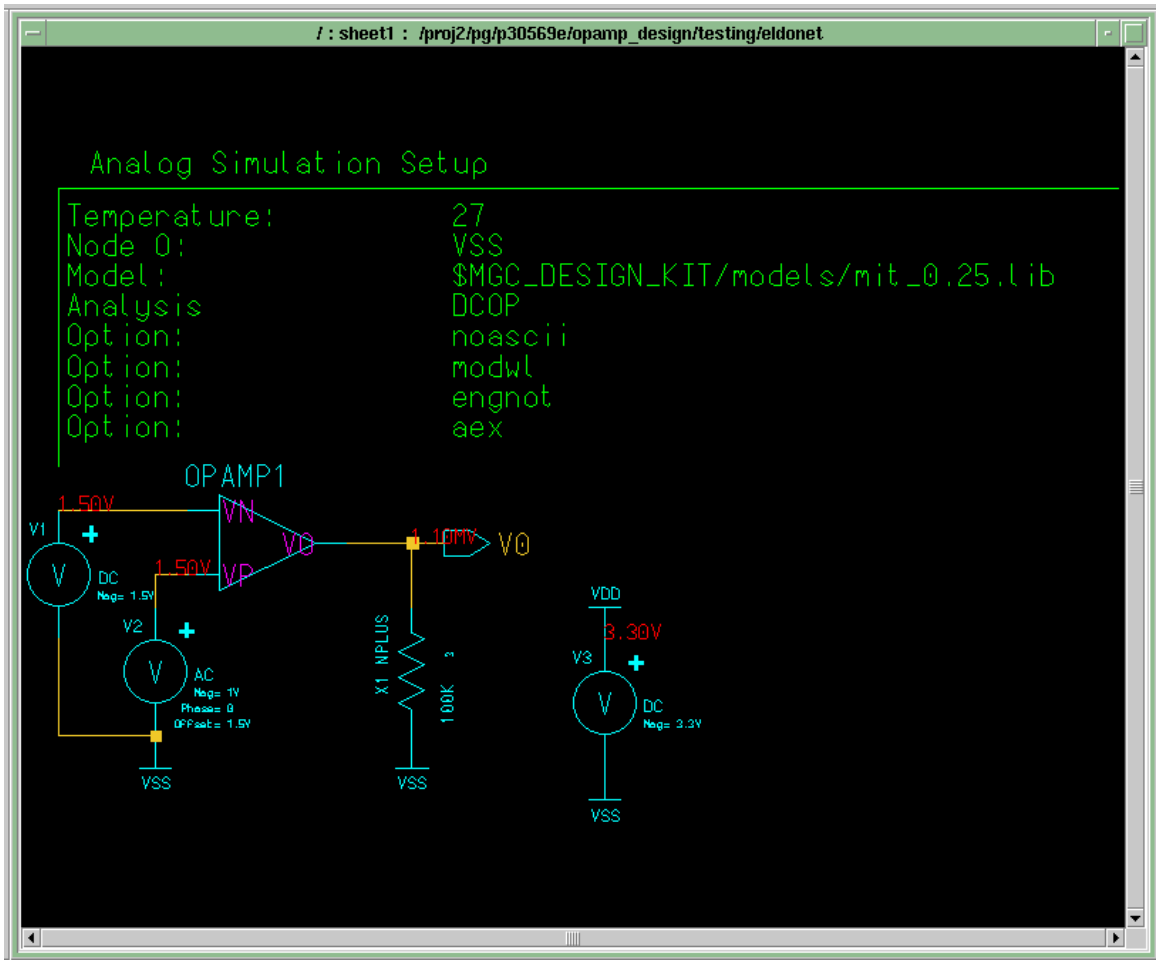
The gain in dB and phase of the opamp are shown in Xelga.


Xelga 3.9_3.1
Control View Page Graph Wave DSP Font Style Globals Help
2-Aug-2004 File : testing_eldonet.cou
16:37:28 ELDO v6.3_1.1 (Production version) : * Component: /proj2/pg/p3
dB VDB(V0)
-220
-230
-240
-250
-260
-270
-280
-290
-300
-310
1e+06
1e+07
1e+08
1e+09
Hz
deg VP(V0)
180
150
100
50
0
-50
-100
-150
-180
1e+06
1e+07
1e+08
1e+09
Hz

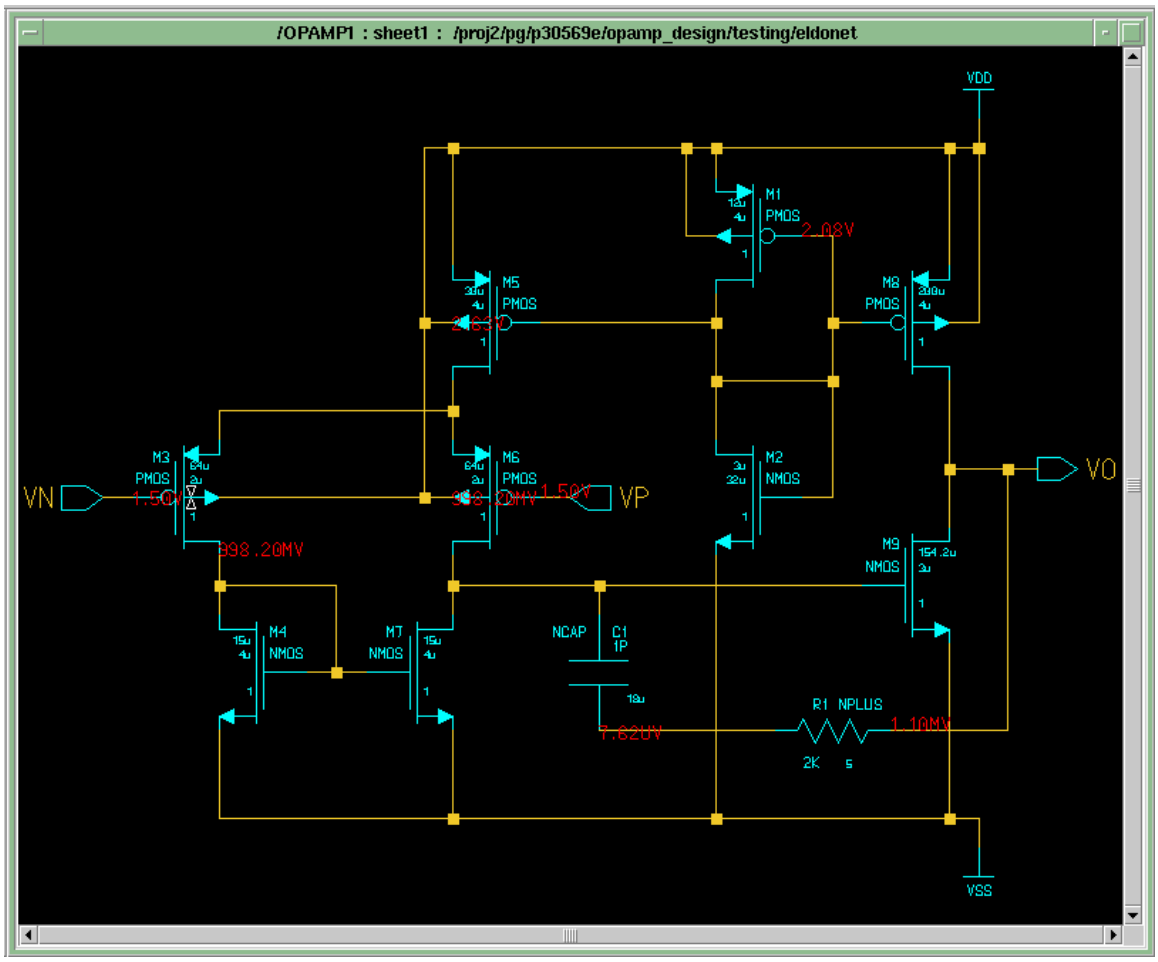
5.4 DC Analysis

Click ***Setup*** > ***Analyses***, enable **DCOP** and disable AC. Then click ***Setup*** > ***Wave Outputs*** > ***Edit***, remove all previously saved items.

See the changes shown in the settings block. Then click ***Execute*** > ***Run ELDO***. Check if there are any errors in the popup windows. After simulation, click ***Results*** > ***DCOP/TRAN>Show Voltage***. All DC operating voltages are shown in the schematic window.



Draw the stroke by placing the cursor over the opamp instance, then pressing and holding down the middle mouse button as you move the cursor vertically down. Ensure that the start of the stroke is over the opamp symbol. The length of the stroke is not really important but make sure that it is at least an inch long. You will see all DC operating points in the opamp circuit.



5.5 Transient Analysis

End the simulation by clicking "**End Sim**" in the schematic_sim palette.

Change the AC source to a **sin** source, refer to section 4.

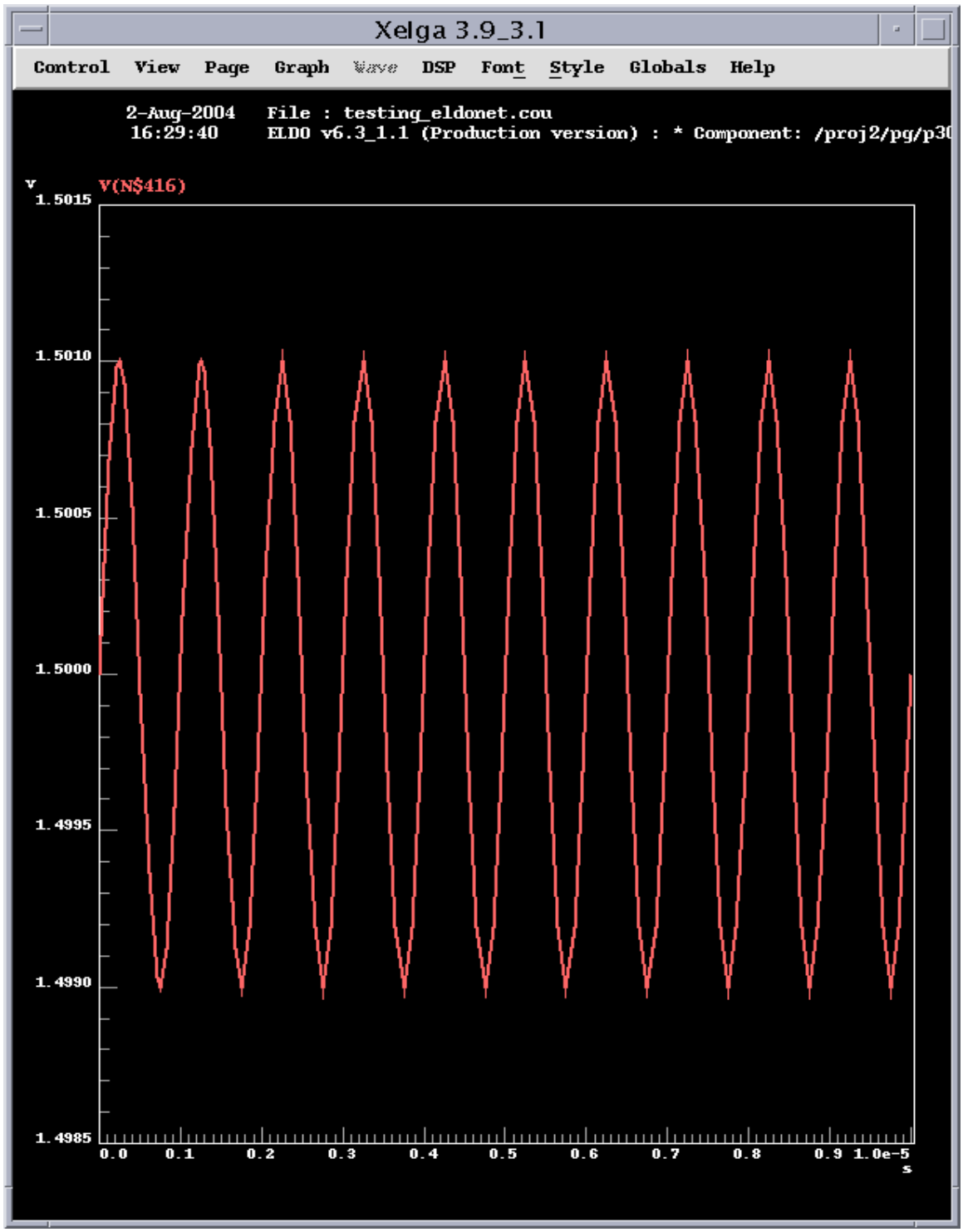
Frequency: 1Meg
ampl: 1mV
offset: 1.5V

and then click **Simulation > Ok** to reenter the simulation mode.

Click ***Setup*** **>** ***Wave Outputs*** **>** ***Edit*** and delete all previously saved items. Click ***Setup*** **>** ***Analyses***, disable DCOP and enable **Transient**. Click Transient Setup and set **Stop time** to be 10u.

Select the line going to **VP** of the opamp and the click ***Setup*** **>** ***Wave Outputs*** **>** ***Save Selected***. Ok the dialog box. Click ***Setup*** **>** ***Session*** **>** ***Show Settings Block*** to verify the simulation settings.

After that, click ***Run ELDO*** to run the simulation and click ***Results*** > ***View Waves*** to view the input waveform to VP of the opamp.



— End of Manual —